Shirazush Salekin Chowdhury

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Summary

- Industrially experienced in the complete flow of Analog Mixed-Signal IC design and verification, including block to top-level design, GDS generation, physical verification (LVS, DRC, EM, IR), and tape-out using commercial EDA tools.
- Experienced in designing high-performance neuromorphic circuits for AI/ML applications.

Research Area

Analog Mixed-Signal Integrated Circuits, Neuromorphic Computing, AI Hardware Accelerator, and In-Memory Computing.

Education

Doctor of Philosophy, Electrical Engineering, Virginia Tech, USA, CGPA: 4.00/4.00 **Aug 2023 — Present**

Coursework: Advanced Analog Integrated Circuits, Advanced Machine Learning.

Master of Science, Electrical and Electronic Engineering, AIUB, Bangladesh, CGPA: 4.00/4.00 **Jun 2019 — Apr 2021**

Coursework: Semiconductor Materials and Hetero-structures, Quantum Phenomena in Nanostructures, Power Electronics.

Bachelor of Science, Electrical and Electronic Engineering, AIUB, Bangladesh, CGPA: 4.00/4.00 **Jan 2016 — May 2019**

Coursework: VLSI Circuit Design, Digital Design I and II, Analog and Digital Circuit Designs, Signals and System, Control Systems.

Academic Experience

Graduate Research Assistant, MICS and BRICC Lab, Electrical Engineering, Virginia Tech **May 2024 — Present**

- Next-generation low-power, high-performance neuromorphic computing solutions.
- RF Integrated Circuits (RFIC).

Graduate Teaching Assistant, Electrical Engineering, Virginia Tech **Aug 2023 — May 2024**

- Conducted courses titled Digital Design - I, and Intro to ECE Concepts.

Industrial Experience

Senior Engineer **Aug 2019 — Jul 2023**

Globalfoundries DTCO (ODC)
Circuit & System Design Department, Ulkasemi Pvt. Ltd. **Dhaka, Bangladesh**

- Analog Circuit Design and Layout.
- Custom Mixed-Signal IC Layout Design.
- Standard Cell Library Development.
- Hardware and Programming: Python, Bash, SKILL, Verilog, Verilog-A, and Verilog-AMS.
- Experienced in industry-standard tools such as Cadence Virtuoso, Spectre, Voltus, and Liberate; Synopsys StarRC, HSPICE, ICC, ICC2; and Mentor Calibre.

Projects

- **Image Classification AI Chip using Delay Feedback Reservoir Computing (DFR) in GF22FDX Technology:** Developed a DFR chip capable of character recognition in 2.03 µs with a power consumption of only 7.5 mW RMS. Achieved classification accuracies of 98.52% on the EMNIST dataset and 99.83% on the MNIST dataset. This chip has been taped out in GF 22FDX SOI technology.
- **Current Project:** High Frequency Analog Front End (AFE) of MEMS indirect Time-of-Flight (iTOF) for Eye Tracking.
  - **Transimpedance Amplifier (TIA):** A 5-GHz inductorless transimpedance amplifier with 77.5 dBΩ gain, utilizing dual-feedback loops and back body biasing, capable of amplifying currents from 100 nA onward.
- **10-bit Successive-Approximation (SAR) ADC:** Developed and optimized a 10-bit SAR ADC with a 100 MS/s sampling rate, achieving 8.72 ENOB and 53.51 dB SINAD, with detailed noise analysis and mitigation across jitter, comparator, and clock phase noise sources.
- **Delta-Sigma Modulator in 55nm Technology [Github]:** The Delta Sigma Modulator, operates at 1.2V, supports 10KHz to 50KHz, uses 600mV reference voltage, 5-10MHz clock speed, 10µA reference current, and has 1-bit resolution.
- **Phase-Locked Loop (PLL) in 22nm and 65nm Technologies [Github]:** Designed a low-power PLL (200 MHz to 1.6 GHz, 1.2V) with 507-873 ns settling time and 110.5-215.3 µW power across PVT variations.
- **Bandgap Reference in 22nm Technology [Github]:** The Bandgap Reference operates at 1.8V, provides 1.06V output, with ±34.3 ppm/°C temp. coefficient, consumes 365.6 µW, and functions from -40°C to 125°C.

Recent Tape-out Experience

- Taped-out an Image Classification AI Chip based on Delay Feedback Reservoir Computing (DFR) using GF22FDX technology. This work includes mixed signal circuit design and custom top level chip layout from scratch.
- High Frequency Analog Front End of MEMS indirect Time-of-Flight (iTOF) for Eye Tracking [Ongoing - expected tape-out in Jan-25]

Selected Publications

1. **Chowdhury, S. S.,** Sarkar, M. R. & Yi, C. Y. *Energy-Efficient Reconfigurable MRAM-Enabled Delay Feedback Reservoir Computing at the Edge.* [Submitted in IEEE TCAS-II]. 2024.
2. Sarkar, M. R. *et al. An In-Memory Power Efficient Computing Architecture with Emerging VGSOT MRAM Device* in *2024 IEEE International Symposium on Circuits and Systems (ISCAS)* (2024), 1–5.
3. **Chowdhury, S. S.** & Arifin, F. *The Effects of the Substrate Doping Concentrations on 6H-SiC Nano-Scale ggNMOS ESD Protection Device* in *2021 2nd International Conference on Robotics, Electrical and Signal Processing Techniques (ICREST)* (2021), 329–333.